



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

K

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/450,802	11/29/1999	JAY SETHURAM	STRAT-P013	8198
33031	7590	11/24/2004	EXAMINER	
CAMPBELL STEPHENSON ASCOLESE, LLP 4807 SPICEWOOD SPRINGS RD. BLDG. 4, SUITE 201 AUSTIN, TX 78759			DUONG, DUC T	
		ART UNIT	PAPER NUMBER	
		2663		

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/450,802	SETHURAM, JAY	
	Examiner	Art Unit	
	Duc T. Duong	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 September 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-11 and 14-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,6,7,9,14,18 and 19 is/are rejected.
- 7) Claim(s) 2-5,8,10,11,15-17 and 20 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

- 11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claim 17 is objected to because of the following informalities: On line 2, the words "at the" is misspelled as "at eh". Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the output" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 6, 7, 9, 14, 18, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishikawa (U.S. Patent 5,748018).

Regarding to claim 1, Ishikawa discloses a source synchronous clocking system (Fig. 3A), comprising a source clock domain in a first network protocol layer 100 (Fig. 3A), comprising a register 101 having a first input D for receiving a data signal (Fig. 3A

col. 4 lines 2-3); a second input CK for receiving a clock signal (Fig. 3A col. 4 lines 3-5), and an output Q (Fig. 3A col. 4 lines 5-8); and a buffer 103 having an input CLK for receiving the clock signal and an output 105 (Fig. 3A col. 4 lines 10-14), said buffer generating a delay t_{b103} that is substantially equivalent to a delay through said register (Fig. 3B col. 5 lines 10-12; noted from the timing diagram the buffer delay t_{b103} is substantially equivalent to the data transfer (register) delay t_D); and a destination clock domain in a second network protocol layer 200 (Fig. 3A), comprising a register 201 having a first input D and a second input CK, the first input of said register of said destination clock domain being coupled to the output of said register in the source clock domain (Fig. 3A col. 4 lines 47-49).

Regarding to claims 6 and 18, Ishikawa discloses a serial termination circuit (Fig. 4A; one of terminating resistor 322 and 326 form a serial termination circuit) for absorbing a reflection generated by the data signal (col. 7 lines 10-16).

Regarding to claims 7 and 19, Ishikawa discloses a parallel termination circuit (Fig. 4A; both terminating resistor 322 and 326 form a parallel termination circuit) for absorbing a reflection generated by the data signal (col. 7 lines 10-16).

Regarding to claim 9, Ishikawa discloses a method for operating a source synchronous clocking system between a first layer and a second layer from a source clock (Fig. 3A), comprising receiving an input clock signal CK in a first clock domain in a first layer 100 (Fig. 3A col. 4 lines 3-5); receiving an input data signal D in the first clock domain in the first layer (Fig. 3A col. 4 lines 2-3); latching the input data signal by triggering the input data signal by the input clock signal (Fig. 3B col. 4 lines 55-62);

delaying the input clock signal by an amount that is equal to the delay in the latching device (Fig. 3B col. 5 lines 10-12; noted from the timing diagram the buffer delay t_{b103} is substantially equivalent to the data transfer (register) delay t_D); and generating an output clock signal 105 and an output data signal 106 in the second clock domain in the second layer 200 (Fig. 3A col. 4 lines 41-47), the output clock signal and the output data signal being synchronized to each other (Fig. 3b col. 4 lines 55-65).

Regarding to claim 14, Ishikawa discloses a method for providing a clock input and a data input synchronously (Fig. 3A), comprising the steps of receiving the clock input CK (Fig. 3A col. 4 lines 3-5); receiving the data input D (Fig. 3A col. 4 lines 2-3); transmitting the clock input to a latching device for triggering the data input (Fig. 3B col. 4 lines 55-62); sending the clock input through a buffer (Fig. 3A col. 4 lines 5-8), the buffer having a delay which is equal to the delay through the latching device (col. 4 lines 10-14); and generating an output data from the latching device that synchronizes with an output clock from the buffer (Fig. 3B col. 4 lines 55-65).

Allowable Subject Matter

6. Claims 2-5, 8, 10, 11, 15-17, 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments filed February 20, 2004 have been fully considered but they are not persuasive. Regarding to Applicant's argument on pages 9-13 with respect

to claims 1, 9, and 14 that Ishikawa fails to teach or suggest for “the buffer generating a delay that is substantially equivalent to a delay though said register”.

In reply, Ishikawa indeed discloses as cited in the previous portion Fig. 3B col. 5 lines 10-12 a timing diagram showing the buffer 103 generating a delay t_{b103} that is substantially equivalent to the data transfer (register) delay t_D .

In the Applicant's argument, Applicant argued that the timing diagram in Fig. 3B is not drawn to scale, the quantity labeled t_{b103} is perceptively smaller than t_D , and thus the Applicant assert there not teaching or suggestion that t_{b103} is “substantially equivalent” to t_D . In contrary to the Applicant's assertion, even with the timing diagram not being drawn to scale and that t_{b103} is perceptively smaller than t_D , t_{b103} is still “substantially equivalent” to t_D . The reason being that the phrase “substantially equivalent” does not have a definite amount or value as to what is consider “substantially equivalent”. Thus, the broadest interpretation is given to the phrase.

In the Applicant's argument, Applicant also argued that all words in a claim must be considered in judging the patentability of that claim against prior art and thus the terms “network”, “protocol”, and “layer” must be consider. Furthermore, Applicant asserted that one skill in the art would recognize the terms are used to provide specific functionality. In response, Examiner would like to point out the features upon which applicant relies (i.e., network protocol layer providing specific functionality) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Additionally with respect to claim 14, Examiner would also like to note the recitation "a link layer and a PHY layer" in lines 2-3 has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

In the Applicant's argument, Applicant stated that Ishikawa fails to teach or suggest "delaying an input clock signal by an amount that is equal to the delay in the latching". In reply, Ishikawa discloses in Fig. 3B col. 5 lines 10-12 a timing diagram showing the buffer 103 generating a delay t_{b103} that is substantially equivalent to the data transfer (register) delay t_D . Herein, Examiner would like to point out the phrase "substantially equivalent" is interpreted as "equivalent". The reason is in order for an invention to be granted of patentability, the invention must show proof that it is better or possesses advantages over the prior art by yielding unexpected results, *In re Skoner*, 186 USPQ 80 CCPA 1975. Thus, unless Applicant shows "delaying an input clock signal by an amount that is equal to the delay in the latching" would yield unexpected results as compared to Ishikawa "delaying an input clock signal by an amount that is substantially equal to the delay in the latching", patentability cannot be granted.

In view of response herein, the rejections are maintained.

Art Unit: 2663

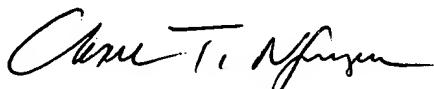
Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Duong whose telephone number is 571-272-3122. The examiner can normally be reached on M-Th (9:00 AM-6:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DD
DD



CHAU NGUYEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600